Low-supply-voltage High-linearity ADC with Dynamic Analog Components

Hao SAN
Dept. of Electrical, Electronics and Communication Eng., Tokyo City University
Tokyo, Japan. Email: hsan@tcu.ac.jp

***Abstract*—This paper presents high-linearity analog-to-digital converter (ADC) techniques with dynamic analog components at supply voltages below 1V. To reduce the complexity of the circuit configuration and minimize the active area of multi-bit ADC for high-resolution, the cyclic ADC consist of a simple analog conversion stage and backend logic circuits is applied. The 1bit/step conversion method is utilized, where each conversion step employs the same conversion stage circuit for analog signal processing, resulting in minimal parameter variation between steps. A non-binary method is also proposed for cyclic ADC, which utilizes the redundancy of non-binary AD conversion to tolerate the analog errors caused by circuit element mismatch and non-ideal characteristics of the amplifier and/or comparator in the analog conversion stage, and thus guarantee the linearity of ADC. The body-voltage-control technique is utilized to decrease the threshold voltage of SOTB CMOS, thereby facilitating the low-voltage operation of the ADC circuit. Dynamic analog components such as amplifiers and comparators are utilized for low-voltage operation, while circuit techniques are developed to improve the DC gain and bandwidth of the amplifier. These improvements further enhance the linearity and speed of the ADC at low-supply-voltage. The experimental results of the proposed non-binary cyclic ADCs show that 14-bit linearity can be achieved at Vdd = 0.9V, demonstrating the feasibility and effectiveness of the proposed circuit techniques for high-linearity ADCs at supply voltages below 1V.**

Keywords— non-binary ADC, Cyclic ADC, dynamic amplifier